Power Electronic Design and Layout Techniques for Improved Performance and Reduced EMI

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Abstract — This paper is a summary of a 75 minute seminar that describes how the physical layout and routing of power electronic circuits affects circuit performance, and influences EMI/RFI generation. Three categories of common circuit board layout effects are presented: impedance effects, capacitively induced effects, and inductively coupled effects. Guidelines are presented to determine the bandwidth of the signals of interest, along with methods for determining appropriate conductor geometries. Capacitor selection for decoupling, bypassing, and snubbing is also discussed. The seminar handout package contains all of the overheads, figures, and examples which are not included in this summary.

INTRODUCTION

The advantages offered by power electronic circuits are making them increasingly prevalent in automotive and other transportation systems. This is evident in the proliferation of converter ICs, driver chipsets, smart-power modules, short-circuit-proof power devices, and so on. While the proper selection of these components is an important part of the design of such systems, an often overlooked design aspect of equal importance is the physical layout and routing of the circuit. Seemingly small amounts of stray capacitance or leakag inductance can have a profound effect on circuit behavior. Poor layout will result in unreliable operation, increased EMI, reduced efficiency, and even device failure.

The first part of this summary covers the reasons why copper tracks on a circuit board do not always behave the way we might expect, and how this can affect circuit performance. Next the interactions between several conductors on a circuit board are discussed, including capacitive and inductive coupling. Finally, capacitor selection for decoupling, bypassing, and snubber circuits is discussed.

EFFECTS DUE TO CONDUCTOR IMPEDANCE

Conductivity and DC Effects

Most engineers are quite familiar with the concepts of conductivity and cross-sectional area, and are able to determine the DC resistance of a copper track. This is clearly a consideration in high-current circuits where copper tracks on a circuit board may be used at tens or even hundreds of amps. The obvious solution to excessive voltage drop is to increase conductivity by widening tracks, increasing copper thickness, paralleling tracks, or reducing track length (or some combination of these). Solutions becomes much less obvious, however, when sensing and feedback loops are involved, and the question arises "which end of this ground track is really ground?" The essence of this problem is that a small voltage drop due to high current flow can add or subtract from a sensitive voltage reference node in the control circuit and introduce significant errors. The high current output and the low-level sensing circuits are essentially sharing a current path. Since the impedance of a track can not practically be reduced to zero, the solution is to think about where the currents flow, and arrange the interconnection so as to reduce the undesirable consequences of the shared current path voltage drop.

IMPEDANCE EFFECTS AT HIGHER FREQUENCIES

Frequency versus Bandwidth

Clearly, track resistance can affect circuit performance, but the situation becomes more complex as signal bandwidth increases. Notice that here we are discussing *bandwidth* rather than frequency. This is because one needs to consider the complete spectrum of a signal, not just it's fundamental frequency. For example, most engineers would consider 50 Hz to be a relatively low frequency. Looking at the frequency spectrum of a 50 Hz square wave produced by an ACT family logic gate, however, we would find significant components beyond 50 MHz! In this example, the bandwidth of the signal can be nearly a million times larger than the fundamental frequency! We can approximate the upper band limit of a signal based on it's risetime:

$$Bandwidth(Hz.) = \frac{0.35}{Risetime(\text{sec.})}$$

So, what does signal bandwidth have to do with track impedance? First of all, we are not talking about *characteristic impedance*, which is a transmission-line concept. In most cases for power electronics, the wavelengths at the highest significant harmonics are more than an order of magnitude longer than any track dimension. We can therefore consider a PC board track as a simple first-order series R·L equivalent circuit, although we will later cover the frequency dependent nonlinearity of the R component.

Geometry Dependence of Inductance

At DC, the impedance of a copper track is simply its resistance as measured by an ohmmeter. As the frequency is increased, however, the self-inductance becomes significant compared to the resistance, and the overall complex impedance Z of the track will begin to rise. Since both the resistance and the self inductance of a track depend on it's geometry, the frequency where this occurs can vary significantly. What's more, some parameters affect only resistance, others affect mostly inductance, and some affect both. For example, doubling the thickness of a copper track will cut the DC resistance in half, but have little effect on the inductance. Doubling the width, however, will reduce the inductance, but only by a factor of approximately the square-root of width increase.

Consider a straight 2.5 mm wide, 35 µm thick copper track 10 cm long. Calculating and measuring the DC resistance is easy, but calculating or measuring the inductance is less straightforward. The reason is because inductance is influenced by the total loop-area in which current flows, and w have so far only defined one 10 cm long section of an verall loop. So, we could define that the far end of the track connects with a via to an "infinite" ground-plane on the opposite side of a 1.6 mm thick board. Now, the inductance can be estimated and measured as approximately 40 nH, and is directly proportional to length (i.e. 4 nH per cm). To put this into perspective, the 40 nH represents an inductive reactance f 2.5Ω at 10 MHz. Now, suppose the ground-plane is shrunk down to a 2.5 mm track directly opposite the original 10 cm track. Surprisingly, the inductance only increases about 25% to 50 nH total. Moreover, if the return-path track is moved to the same side of the board as the original track (so the loop looks like a U with 10 cm long sides, and a 2.5 mm space between the sides) the inductance doubles to slightly more than 80 nH. If the same U were made with 5 mm wide track, the inductance drops to about 57 nH.

There are a variety f circuit layout probl ms which can be attributed to track inductance. In almost all cases, the problem relates to a $V(t) = L\,di/dt$ reaction voltage to an applied current transient. In some cases, th reaction voltage appears as a common-mode voltage, induced by the power stage into a shared current path in the low-power portion of a circuit. The parasitic track inductance in a power circuit will also store energy which must be dissipated each cycle. Oftentimes, this stored energy appears as ringing and overshoot on voltage waveforms, and results in increased power device stresses and increased EMI. Solutions to these types of problems generally involve lowering track impedance and separating current paths on the layout. In addition, routing supply and return currents in a stripline fashion help to reduce radiated emissions.

AC Resistance, Skin and Proximity Effects

You may recall from electromagnetics courses, that at high frequencies current tends to crowd to the surface of conductors. The result is that high-frequency current flowing in the conductor does not use all of the available cross-sectional area, and therefore sees a higher resistance. Like most electromagnetic phenomena, the effect is non-linear, and increases with the square-root of frequency—and gets worse if the conductor has a magnetic permeability greater than air. The standard formula for skin depth in copper is given below.

$$\delta = \frac{6.61}{\sqrt{f}} \text{ (units are in cm and Hz.)}$$

The skin depth only tells us how far below the surface f a conductor the current density has decreased to 37% of its value at the surface. What we really want to know is what the resistance versus frequency curve looks like for various copper thicknesses. The answer depends on the proximity of the return-path of the conductor. This additional dependence, known as the proximity effect, is well-known by transformer designers. The proximity effect accounts for how current-carrying conductors induce skin effects in neighboring conductors. The proximity effect is generally thought f in terms of worsening the problems of skin effect, but this is nly the case when the neighboring conductors are carrying current in the same direction.

This would be the case if for example copper tracks were paralleled on several layers of a circuit board to carry high current in one direction. Proximity effects would increase the AC resistance of each layer as a result of interaction with the others. If alternate layers on the board was carrying the return current, however, the proximity effect would be dramatically reduced. This is similar to interleaving the primary and secondary windings on a transformer to reduce leakage inductance. In the interleaved conductor example, the H fi ld is much more compact, and the capacitance between supply and return current paths is increased. The reduced magnitude f the external H field can also help to reduce radiated emissions. The interleaved structure just described would be an excellent topology for a DC bus.

One other important c ncept to remember related t skin effect is that thicker copper will always result in lower resistance at a particular frequency, but not in proportion to the thickness increase. Instead, it is more effective to choose the copper thickness which has an AC/DC ratio less than 1.5, and make the track wider to achieve the desired low impedance, since c nductivity follows width linearly.

CAPACITIVELY INDUCED EFFECTS

The planar structure of a circuit board, particularly in combination with wide copper tracks used in power electronics, can lead to significant capacitive coupling between circuit nodes. While there are situations where this might be desirable—a DC bus for example, there are plenty of other situations where this coupling is undesirable. More often than not, the problems originate when auto-routing software is allowed to lay out a circuit board. A typical scenario is that a high impedance input node is routed through a power stage where fast transient voltages occur. For example, a CMOS gate-driver input might be routed under a high-side FET source in a half-bridge system. When the high-side FET turns on, the source *dv/dt* can easily be greater than 10 volts/ns. Even if the coupling capacitance is only 5 pF, the peak current induced in the gate driver input is 50 mA. Since CMOS gate driver chips are usually set-up to be TTL compatible, they often have threshold voltages in the 1 to 2 volt range. Therefore, the impedance of the circuit driving the CMOS input must be less than 20 to 40 ohms in order to prevent the capacitively coupled voltage spike from being interpreted as an asserted logic signal. Since the input side of drive circuits typically have impedances several orders of magnitude higher than this, one can see that stray capacitance values which might appear insignificant can in fact be quite a problem.

The result of this coupling could be multiple switching edges or even oscillation of the high-side switch, creating additional switching loss and EMI. If the coupling were to the low-side driver, a high-current shoot-through condition could occur, possibly causing shutdown or damage to the switch. Clearly this is an undesirable situation that should be avoided during the circuit board layout process.

Capacitive coupling problems can be identified during troubleshooting as positive and negative going spikes superimposed on the signal of interest. These spikes represent a differentiated version of the signal causing the interference. Although the problem manifests itself as a voltage spike, it is really the *C(dv/dt)* current spike times the source impedance that causes the v ltage you see on th scope.

INDUCTIVELY COUPLED EFFECTS

Inductive coupling between two conductors occurs when time-varying magnetic flux generated by time-varying current in one conductor links to an adjacent conductor. This flux generates an emf with a magnitude and direction given by Faraday's law:

$$V_{induced} = -\frac{d\phi}{dt}$$

The geometric relationship between the two conductors, the overall loop-area, and the magnitude of the current determine the total flux linked. The time rate-of-change of the current determines the magnitude of the effect. A typical scenario of an inductive coupling problem is when a track carrying wide bandwidth current in the power stage runs parallel to a low-level signal line in the control circuit. The high current conductor may even be at ground potential, so capacitiv coupling would not necessarily be a concern. Moreover, the low-level signal line may be relatively low impedance; With inductive coupling, a *voltage* is induced rather than a current, and the magnitude of the voltage is relatively independent of the impedance of the receiving circuit.

For example, many control ICs have a current sense input which is typically used to measure switch current from a sense resistor or some other transducer. The current sense inputs typically have very low voltage sensing thresholds on the order of a few hundred millivolts. If the circuit board track from the sense resistor to the control IC is long, and if it happens to run parallel to a high-current carrying conductor, significant errors can be introduced. At first glance, the induced voltage may look like a capacitively induced problem because it appears differentiated. The clue to which type of coupling is involved is whether the interference is a differentiated version of a voltage or a current waveform; A differentiated voltage waveform is the result of capacitiv coupling, and a differentiated current waveform is due to inductive coupling.

There are several possible solutions to inductive coupling problems. The first is to arrange the high-current track so that its return current flows directly under it in the opposite direction. This will minimize the radiated flux causing the problem. The second step is to physically separate the input node from the high current conductor, since the flux density falls off with the square of distance. Ground-planes or copper shield planes will act as eddy-current shields, and may be somewhat effective at attenuating the radiated flux, but the other solutions should be implemented first.

CAPACITORS FOR POWER ELECTRONIC CIRCUITS

By reducing the high frequency impedance of the tracks on a power circuit board as discussed earlier, significant improvements in performance can be realized. This is only true, however, if the circuit board tracks represent the dominant impedance in the system. It is quite possible that the parasitic and packaging impedance of the components themselves is the dominant impedance. This is true of every component on the board, but we will pay particular attention to capacitors, since they are commonly a major source of parasitic impedance.

Capacitors for Decoupling and Bypassing

Capacitors play an important role in maintaining a stable, smooth supply voltage to the various control and driver ICs used in power electronic circuits. A good example of this is a FET or IGBT gate-driver IC. A gate-driver may have low current consumption on average, but delivers high peak currents to charge and discharge the gate rapidly. If the driver IC draws this current from the distribution bus on the circuit board, the resulting *di/dt* times the track inductance will likely disturb other ICs on the bus, subjecting them to a glitch on their supply voltage. Capacitors are therefore used as a local energy reservoir right next to the IC so that the fast current spikes are supplied from the capacitor rather than the distribution bus. These capacitors are called *bypass* or *decoupling* capacitors.

In order for the bypass capacitor to be effective, it must have a low impedance relative to the distribution bus. In the ideal sense, this simply means choosing a capacitor with a large value. In the real-world, however, bigger is not necessarily better. It is more important to select a capacitor based on its impedance rather than its overall capacitance for this application.

For example, electrolytic capacitors typically have large capacitance values in a small package, but do not have low Effective Series Resistance, or ESR. Moreover, the manufacturing technique often results in a significant inductance. If you plot the total impedance Z versus frequency, you will see that at low frequencies, the capacitance dominates the overall impedance. As the frequency is increased, the capacitor will approach series self-resonance, which will show up as an impedance minimum. Above this resonance, the self-inductance dominates, and the impedance goes back up again. The impedance value at resonance represents the ESR of the capacitor.

Tantalum dielectric electrolytic capacitors typically have lower ESR than similar valued aluminum electrolytics, and are usually smaller. Their main drawback is relatively high cost.

Ceramic capacitors come in a variety of different dielectric materials that have different energy densities and temperature coefficients. Ceramic capacitors generally have lower ESR than electrolytic types, but different construction techniques among ceramic types can have significant effects on performance. It is best to measure a candidate capacitor on an impedance analyzer to determine its suitability.

Film dielectric capacitors like polyester, polypropylene, polystyrene, and polycarbonate are manufactured with metallized film, or film and foil construction techniques. These capacitors typically have excellent ESR characteristics. Different wrapping arrangements and lead-out configurations will affect the impedance, so special low-inductance, low-ESR types should be specified where needed. The downfall of film capacitors is their relatively low energy density (large size for small capacitance).

Selecting an appropriate capacitor for bypassing does not necessarily mean having to choose giant film capacitors or expensive Tantalums just to get the required capacitance and low ESR. One common solution is to use a parallel combination of an electrolytic and ceramic or film capacitor. The electrolytic provides the energy storage and low frequency requirements, and the smaller valued ceramic capacitor provides the low impedance at higher frequencies.

Capacitors for DC Bus and Snubbing

The same general rules of thumb apply to capacitors used on a DC bus. In bridge circuits, the high frequency bypass capacitors on the DC bus are often referred to as snubber capacitors. There are generally two needs that must be met for DC bus applications. First is the total energy storage requirement. For this purpose, large aluminum electrolytic capacitors are used. Special versions are available which have been optimized for high ripple current and low ESR applications. Even then, it is usually necessary to add parallel high frequency bypass capacitors.

Some of the film capacitors are available with extremely low impedance in values up to several microFarads. These types generally have flat copper beam-leads for lowest impedance interconnection. One other type which has excellent performance at higher voltages are silvered mica capacitors. Although they are extremely low ESR and inductance, their maximum capacitance is generally limited to about 10 nF. Film or mica capacitors are also excellent choices for RC or RCD snubber circuits, due to their low impedance and low dissipation factor.